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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	:	Seung-Hwan Oh		
SERIAL NO.	:	09/473,846	EXAMINER	: Anne L. Damiano
FILED	:	December 28, 1999	ART UNIT	: 2114
FOR	:	METHOD FOR PROCESSING ERROR OF RECEIVED PACKET IN ETHERNET MAC LAYER		

APPEAL BRIEF TRANSMITTAL LETTER

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

Dear Sir:

Appellants respectfully submit three copies of a Brief For Appellants that includes an Appendix with the pending claims. The Appeal Brief is now due on September 1, 2004.

Appellants enclose a check in the amount of $330.00 covering the requisite Government Fee.

Should the Examiner deem that there are any issues which may be best resolved by telephone communication, kindly telephone Applicants undersigned representative at the number listed below.

Respectfully submitted,

By: Steve Cha
Attorney for Applicant
Registration No. 44,069

Date: September 1, 2004

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Steve Cha, Reg. No. 44,069
(Name of Registered Rep.)

(Signature and Date)

OIPE JC166
SEP 0 3 2004
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Seung-Hwan Oh**
Application No.	:	**09/473,846**
Filed	:	**December 28, 1999**
For	:	**METHOD FOR PROCESSING ERROR OF RECEIVED PACKET IN ETHERNET MAC LAYER**

APPEAL BRIEF

On Appeal from Group Art Unit 2114

Date: September 1, 2004

Steve Cha
Attorney for Applicant
Registration No. 44,069

Certificate of Mailing Under 37 CFR 1.8

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Steve S. Cha, Reg. No. 44,069
(Name of Registered Representative)

(Signature and Date)

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, Samsung Electronics, Co., Ltd., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-4 have been presented for examination. All of these claims are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

An amendment after-final was filed in the Patent Office on June 29, 2004. As the amendment clearly explains in the second paragraph of the REMARKS section, the amendment merely adopts the claim revision for claims 1-3 suggested by the Examiner, without modifying, or adding to, the claims in any other way. The Examiner suggests the revision in objecting to claims 1-3 in the final Office Action mailed January 29, 2004. No Advisory Action was received in response to the June 29, 2004 amendment. In an August 12, 2004 phone call, the Examiner refused to issue an Advisory Action.

Items 1-3 of the January 29, 2004 final Office Action state:

> 1. Claim 1 is objected to because of the following informalities: Line 7, "the error packet" lacks antecedent basis. Line 8, "the entire error packet" lacks antecedent basis. These are interpreted as meaning the packet in which the error is detected. Appropriate correction is required.
> 2. Claim 2 is objected to because of the following informalities: Line 8, "the error packet" lacks antecedent basis. Line 9, "the error packet lacks antecedent basis. Line 10, "the entire error packet" lacks antecedent basis. These are interpreted as meaning the packet in which the error is detected. Appropriate correction is required.
> 3. Claim 3 is objected to because of the following informalities: Line 3, "the error packet" lacks antecedent basis. This is interpreted as meaning the packet in which the error is detected. Appropriate correction is required.

The instant APPENDIX is divided into two sections. Section A shows the claims as they appeared on record prior to the June 29, 2004 after-final amendment. Section B shows the claims as they appear in the June 29, 2004 after-final amendment.

Referring to section B, the claims merely adopt the Examiner's suggestion set forth in the above-quoted items 1-3 of the final Office Action. Accordingly, if the June 29, 2004 after-final amendment has not been entered, it is unclear on what grounds. MPEP 714.13(II), second paragraph. As mentioned above, the Examiner refuses to respond with an Advisory Action.

In the analysis below, we assume that the June 29, 2004 after-final amendment has not been entered.

A prior after-final amendment was filed on April 27, 2004 which incorporated the same revision to claims 1-3 and an additional modification to the claims. The April 27 amendment was refused entry on the basis of requiring further search and consideration.

V. SUMMARY OF THE INVENTION

To reduce time overhead (page 8, lines 6-10) in processing an erroneous packet incoming to an Ethernet station or "node" under the IEEE 802 standard (page 2, lines 12-13), storage of the packet at the medium access control (MAC) layer (FIG. 1, ref. no. 50) and transmission of the stored packet to the next stage, e.g., switch (FIG. 1, ref. no. 60), is stopped upon detection of the error (FIG. 1, ref. no. 40; page 5, lines 19-21). The present invention applies to a packet exceeding a predetermined size, e.g., 64 bytes in length (page 2, lines 17-22).

In the prior art, if the incoming packet is detected as erroneous while being received at the MAC layer from the physical layer and does not exceed 64 bytes in length, the prior art IEEE 802 standard discards the erroneous packet. If, however, and in contrast to the present invention, an error is detected in a packet exceeding 64 bytes in length, the MAC layer receives the entire packet and then transmits the packet to the switch, along with an error signal (page 2, lines 4-22).

The present invention saves the time that would otherwise be wasted in transmitting the entire erroneous packet to the switch (page 2, lines 19-22).

In one aspect according to the present invention, upon detection of an error while receiving the packet from the physical layer, storage of the packet in a memory and transmission of the packet to the switch are stopped, and the error and end-of-packet signals are transmitted to the switch (page 3, lines 17-21). Stoppage occurs without waiting for a complete reception of the entire erroneous packet (page 8, lines 4-6).

In another aspect according to the invention, upon detecting an error while transmitting to the switch the packet received from the physical layer, transmission of the

erroneous packet to the switch is stopped, and the error and end-of-packet signals are transmitted to the switch. Stoppage occurs without waiting for a complete reception of the entire erroneous packet (page 7, lines 6-13).

VI. ISSUES

A. Whether claim 1 is unpatentable as anticipated under 35 U.S.C. 102(e) by U.S. Patent No. 5,999,538 to Haddock et al. ("Haddock").

B. Whether claims 2 and 3 are unpatentable as obvious under 35 U.S.C. 103(a) over the prior art disclosed in the applicant's application (hereinafter "PAAA") in view of U.S. Patent No. 5,493,562 to Lo.

C. Whether claim 4 is unpatentable as obvious under 35 U.S.C. 103(a) over PAAA in view of Lo and U.S. Patent No. 6,295,281 to Itkowsky et al. ("Itkowsky").

VII. GROUPING OF CLAIMS

Claims 2 and 3 stand or fall together. Claim 1 stands or falls separately. Claim 4 stands or falls separately.

VIII. ARGUMENT

A. CLAIM REJECTIONS UNDER 35 U.S.C. 102(e)

Claim 1 recites:

> receiving a packet from the physical layer and transmitting the packet to a switch;
> detecting for an error while transmitting the packet;
> upon detection of the error, stopping the transmission of the error packet to the switch without waiting for a complete reception of the entire error packet; and

> transmitting a signal indicating an occurrence of the error and a signal indicating an end of the packet to the switch.

Firstly, the Office Action does not specify what is deemed in Haddock to correspond to "transmitting the packet to a switch." The only switch disclosed or suggested in Haddock is a node that happens to be a switching hub (col. 6, line 29: "switching hub"). Judging from the paragraph at the top of page 4 of item 5 of the Office Action, this appears to be the sense in which the Office Action is hoping to find a switch in Haddock.

Item 5 on page 4 of the Office Action cites in Haddock lines 6, 16-25, 28-30, 36-38, and 49-58 of column 2. The Office Action states:

> Since more than one node knows when a packet collision has occurred, some sort of signal must be present in the system to indicate the occurrence of an error. Since the jam signal is sent for a period of time, immediately prior to the stopping of transmission, it is interpreted as being an end of packet signal. Immediately following the detection of error, the jam signal is sent for a period of time, however, the node still stops transmitting without waiting for a complete reception of the entire packet.

According to the above explanation by the Office Action, the detecting step of the present invention as recited in claim 1 corresponds to checking, by a Haddock node (col. 6, line 36: "node"; col. 2, lines 7-9: "nodes") for the presence of a carrier signal under a CSMA/CD protocol (Haddock, col. 6, line 39) while that node is transmitting the packet (Haddock, col. 6, lines 49-53; col. 1, lines 45-47). The detecting step of the present invention explicitly says, "detecting for an error while transmitting the packet."

However, while checking for the presence of a carrier signal, transmission occurs at the physical layer (Haddock, col. 6, lines 40-41: "transmitting on the communication medium"), and "the packet" to be transmitted by the Haddock node on the physical layer is received from an upper layer. The physical layer, which by definition is the lowest

layer, relates to the communication medium, e.g., electrical wire, whereas data or information to be sent by node the Haddock node onto the medium inherently arrives from an upper layer, such as the MAC sub-layer.

By contrast, the receiving step of the present invention as recited in claim 1 specifies, "receiving a packet from the physical layer and transmitting the packet to a switch." The reference in the receiving step to "a packet" necessarily refers to the same packet later referred to as "the packet." Accordingly, at least since the Haddock packet to be transmitted at the physical layer is received from an upper layer, it is unclear how Haddock can fairly be said to disclose, "receiving a packet from the physical layer and transmitting the packet to a switch; detecting for an error while transmitting the packet . . ." which language explicitly appears in claim 1 of the present invention.

Item 5 at page 3 of the Office Action states, "In an Ethernet, packets are received by the MAC layer from a physical layer," but this explanation ignores the scenario the Office Action is offering. The Office Action suggests that the detecting step of claim 1 corresponds to detecting, by the Haddock node, for the presence of a carrier signal while that Haddock node is transmitting at the physical layer. However, the Haddock packet to be transmitted is received from an upper layer. Accordingly, Haddock cannot be characterized as receiving that packet "from the physical layer and transmitting the packet to a switch; detecting for an error while transmitting the packet" which language explicitly appears in claim 1 of the present invention.

Nor can the Office Action find refuge in citing to the prior art in applicant's application so as to accord correspondence between "switch" in claim 1 of the present

invention and "switch" as the word is used in line 18 of page 2 of the applicant's specification.

Firstly, claim 1 of the present invention receives "a packet" from the physical layer, transmits "the packet" to a switch, detects for an error while transmitting, and, upon detecting an error, stops transmitting "the error packet to the switch." It is unclear to the applicant how the Examiner can use the term "switch" in the sense it is used in the applicant's specification in applying an anticipation rejection based on Haddock.

Moreover, citation to the PAAA in this anticipation rejection is improper, at least because line 18 of page 2 of the present specification says, "the next stage (e.g., switch)." The Examiner would be in the stance of suggesting that the packet being transmitted to the next stage is inherently being transmitted to a switch, which proposition is neither disclosed nor suggested by the PAAA.

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) MPEP 2131.
>
> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) MPEP 2112.

For at least all of the above reasons, Haddock fails to anticipate the invention as recited in claim 1.

B. CLAIM REJECTIONS UNDER 35 U.S.C. 103(a)

1. Rejection of claims 2 and 3

Claim 2 recites:

> receiving a packet from the physical layer, storing the received packet in the memory, and transmitting the received packet to the switch;
> detecting for error while receiving the packet;
> upon detection of the error, stopping the storage of the error packet in the memory and the transmission of the error packet to the switch without waiting for a complete reception of the error packet; and,
> transmitting a signal indicating an occurrence of the error and a signal indicating an end of the received packet to the switch

Item 7 of the Office Action, in the first paragraph at the top of page 6, acknowledges that the PAAA does not disclose or suggest "transmitting a signal indicating an occurrence of the error and a signal indicating an end of the received packet to the switch," but suggests that lines 15-22 of page 2 of the present application constitute PAAA that discloses the receiving, detecting and stopping steps of claim 2 of the present invention.

The applicant submits, however, that none of the prior art disclosed in the applicant's specification discloses or suggests the stopping step. In particular, there is no disclosure or suggestion of "upon detection of the error, stopping . . . the transmission . . . to the switch" which language explicitly appears in claim 2 of the present invention.

Page 2 of the applicant's specification, starting at line 4, explains error processing at an Ethernet station or node of two types of packets received, those consisting of 64

bytes or less and those consisting of more than 64 bytes. The short packet, i.e., having 64 or fewer bytes, is discarded by the node if an error is detected while the node receives the packet. The long packet, i.e., having more than 64 bytes in length, by contrast, is retained even if an error is detected. Moreover, the node receives the entire long packet and transmits the received packet to the next stage (e.g., switch).

Firstly, the only stopping mentioned in the PAAA applies to a packet not exceeding 64 bytes in length, i.e., a short packet, but the PAAA does not disclose or suggest that a short packet is sent to a switch. For example, there is no disclosure or suggestion that a short packet for which no error is detected is transmitted to a switch. For at least this reason, there is no disclosure or suggestion of "upon detection of the error, stopping . . . the transmission . . . to the switch" which limitation explicitly appears in the language of claim 2.

The Lo reference cannot make up for this shortcoming in the PAAA, at least because Lo fails to disclose or suggest, for either the long or short packet, "upon detection of the error, stopping . . . the transmission" which limitation explicitly appears in claim 2 of the present invention. Lo, in fact, will not stop storing information from the erroneous packet at least until the desired information is extracted (col. 4, lines 55-56).

It is concluded from the above analysis that Lo and the PAAA fail to disclose or suggest, alone or in combination, error processing of a long packet which features "upon detection of the error, stopping . . . the transmission of the error packet" which limitation explicitly appears in claim 2 of the present invention.

According to the above, although the Office Action attempts to modify the PAAA to incorporate the feature of "transmitting . . . an end of the received packet to the

switch," the Office Action is confined to attempting this for the special case of a short packet.

It is unclear, however, what motivation would have existed to modify the PAAA to feature, upon detecting an error for a short packet, "transmitting . . . an end of the received packet to the switch."

On the one hand, to conform transparently with the prior-art, IEEE 802 standard (present specification, page 2, lines 12-13), the present invention sends, to the switch, the end-of-packet the switch is expecting for an erroneous, long packet, i.e., a packet exceeding 64 bytes in length (page 2, lines 17-18). The switch is expecting this end-of-packet, because the prior art standard entails sending the entire erroneous packet to the switch, including the end-of-packet.

On the other hand, since the IEEE 802 standard discards the erroneous short packet, the applicant fails to see any reason for sending the switch, in the event of an erroneous short packet, "a signal indicating an end of the received packet" which limitation appears explicitly in claim 2 of the present invention.

The applicant likewise notes that the IEEE 802 packet-error-processing protocol described in the PAAA applies to an Ethernet (present specification, page 2, line 4: "Ethernet") node or station in an Ethernet network, and not to a repeater in an Ethernet network.

Lo, by contrast, is directed to use of a repeater, as "a convenient place to gather error statistics for network management" (Lo, col. 1, lines 35-38), for parsing relevant information from an erroneous packet for storage so that another processor can subsequently examine the information and related statistics. It is unclear what motivation

would have existed to off-load the Lo functionality from its "convenient place" to make an unfounded revision of the IEEE 802 standard. Moreover, as set forth above, it is unclear why, even if such off-loading were to occur, there would be any motivation to transmit to the switch "a signal indicating an end of the received packet" for a short packet.

For at least all of the foregoing reasons, the proposed combination of alleged prior art fails to render obvious the invention as recited in claim 2.

Claim 3 depends from claim 2, and is deemed patentable over the cited references for at least the same reasons set forth above with regard to claim 2.

2. Rejection of claim 4

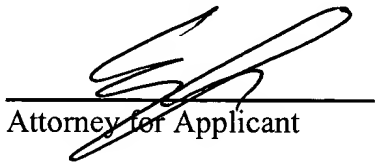
Claim 4 depends from claim 2. The Itkowsky reference discloses the use of FIFOs in an Ethernet repeater, but cannot make up for the deficiencies in the references applied in rejecting claim 2 of the present invention. Accordingly, the proposed combination of references fails to render obvious the invention as recited in claim 2.

IX. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Respectfully submitted,

Steve S. Cha
Registration No. 44,069



Date: September 1, 2004

Attorney for Applicant

X. APPENDIX: THE CLAIMS ON APPEAL

A. VERSION WITHOUT AMENDMENT AFTER FINAL

1. A method for processing a packet exceeding a predetermined size received from a physical layer by a MAC (Medium Access Control) layer of an Ethernet to be transmitted to a switch, the method comprising the steps of:

receiving a packet from the physical layer and transmitting the packet to a switch;

detecting for an error while transmitting the packet;

upon detection of the error, stopping the transmission of the error packet to the switch without waiting for a complete reception of the entire error packet; and

transmitting a signal indicating an occurrence of the error and a signal indicating an end of the packet to the switch.

2. A method for processing a packet exceeding a predetermined size received from a physical layer by a MAC layer of an Ethernet, wherein the received packet is stored in a memory for an eventual transmission to a switch, the method comprising the steps of:

receiving a packet from the physical layer, storing the received packet in the memory, and transmitting the received packet to the switch;

detecting for error while receiving the packet;

upon detection of the error, stopping the storage of the error packet in the memory and the transmission of the error packet to the switch without waiting for a complete reception of the error packet; and,

transmitting a signal indicating an occurrence of the error and a signal indicating an end of the received packet to the switch.

3. The method as claimed in Claim 2, wherein the method further comprising the step of preparing to receive a next packet from the physical layer after receiving the error packet.

4. The method as claimed in Claim 2, wherein said memory comprises a FIFO (First-In, First-Out) memory.

B. AFTER-FINAL AMENDMENT VERSION (as per Section IX above)

1. (Currently Amended) A method for processing a packet exceeding a predetermined size received from a physical layer by a MAC (Medium Access Control) layer of an Ethernet to be transmitted to a switch, the method comprising the steps of:

receiving a packet from the physical layer and transmitting the packet to a switch;

detecting for an error while transmitting the packet;

upon detection of the error, stopping the transmission of the ~~error~~ packet in which the error is detected to the switch without waiting for a complete reception of the entire ~~error~~ packet in which the error is detected; and

transmitting a signal indicating an occurrence of the error and a signal indicating an end of the packet to the switch.

2. (Currently Amended) A method for processing a packet exceeding a predetermined size received from a physical layer by a MAC layer of an Ethernet, wherein the received packet is stored in a memory for an eventual transmission to a switch, the method comprising the steps of:

receiving a packet from the physical layer, storing the received packet in the memory, and transmitting the received packet to the switch;

detecting for error while receiving the packet;

upon detection of the error, stopping the storage of the ~~error~~ packet in which the error is detected in the memory and the transmission of the ~~error~~ packet in which the error

is detected to the switch without waiting for a complete reception of the ~~error~~ packet in which the error is detected; and,

transmitting a signal indicating an occurrence of the error and a signal indicating an end of the received packet to the switch.

3. (Currently Amended) The method as claimed in Claim 2, wherein the method further comprising the step of preparing to receive a next packet from the physical layer after receiving the ~~error~~ packet in which the error is detected.

4. (Original) The method as claimed in Claim 2, wherein said memory comprises a FIFO (First-In, First-Out) memory.